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Enclosed herewith please find the following documents in the above-identified application for United States Letters Patent:

30 Pages of Specification including Abstract and Claims  
20 Numbered Claims Calculated as 20 Claims for Fee Purposes  
5 Sheets of Drawing Containing Figures 1 to 5c.  
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# A VIDEO CODE PROCESSING METHOD, WHICH CAN GENERATE CONTINUOUS MOVING PICTURES

## Background of the Invention

### 5    1. Field of the Invention

          The present invention relates to a method and  
apparatus for processing a video code, which can  
receive, as a original bit stream, a bit stream  
constituted by a video code, which is a digitized  
10    video signal, and then output any one of the original  
bit stream and a converted bit stream into which the  
original bit stream is code-converted. More  
particularly, the present invention relates to a  
method and apparatus for processing a video code,  
15    which can switch smoothly without disturbing a decoded  
picture when switching between the original bit stream  
and the converted bit stream.

### 2. Description of the Related Art

20           Conventionally, in this method for processing a  
video code, when a picture data serving as a video  
signal is encoded to generate a bit stream, a  
transcoding for converting a rate of the bit stream  
into a lower rate is carried out in order to reduce a  
25    band of a transmission path or a memory capacity.

          For example, in a case of a standard type MPEG2  
to compress or expand a color moving picture, a bit

stream is transmitted as a transport stream from a transmission side through an antenna or a network to a reception side. If a band of the antenna or the network is low, the transmission side converts the transport stream into another transport stream of a lower rate. That is, the transmission is done after the execution of the transcoding.

When the reception side records the transport stream, there may be the limitations, such as an upper limit of a bit rate caused by a recorder or a record medium, an upper limit of a capacity and the like. The performance as a memory capacity of a recorder can be improved if the transport stream is converted into the transport stream of the lower rate when it is recorded, namely, if it is recorded after the execution of the transcoding.

Although there may be various methods for the transcoding, it can be attained by a combination of a decoder and an encoder as a simple method. In short, a bit stream is inputted to the decoder, and completely decoded. An output picture data is inputted to the encoder to then generate and output a bit stream of a desirable rate. However, this method carries out the processes for decoding and encoding the bit stream. Thus, the output bit stream is more delayed than the input bit stream by a time necessary for the respective decoding and encoding processes.

For example, in a case of a compression method using a correlation between frames such as the MPEG2, a time delay is induced because of a rearrangement of the frames. That is, a bidirectionally predictive

5 encode picture (B picture) is accumulated in the bit stream in an order different from a picture display order. In a case of a typical MPEG2 stream of [M=3], when the decoding process is done, it brings about a delay corresponding to three frames. Moreover, even  
10 when the encoding process is done, it brings about a delay corresponding to three frames since it waits for an intra encode picture (I-picture) and a predictive encode picture (P-picture).

That is, the bit stream on which the  
15 transcoding is performed has the delay corresponding to six frames with respect to the input original bit stream. For this reason, the simply switching operation between the original bit stream and the bit stream on which the transcoding is performed causes  
20 the moving picture to be discontinuous. Switching between them by omitting the rearrangement of the frames so as not to bring about the time delay results in the disturbance of a screen since the decoding and encoding processes are not carried out normally.

25 Here, the method for perfectly decoding by using the decoder has been already described as the method for the transcoding. However, as another

attaining method, for example, even a method for decoding up to a DCT (Discrete Cosine Transformation) area and again encoding and the like bring about the situation similar to the above-mentioned situation

5 since the bit stream on which the transcoding is performed has the delay with respect to the original bit stream.

Conventionally, there are the proposals of the techniques with regard to a buffer control and a rate control of a bit stream itself on which the transcoding is performed. However, there is no information corresponding to a control with regard to a time difference between the original bit stream and the bit stream on which the transcoding is performed.

10  
15 The above-mentioned conventional method and system for processing the video code have the problem that they can not generate the continuous moving pictures when switching from the bit stream on which the transcoding is performed to the original bit stream, or from the original bit stream to the bit stream on which the transcoding is performed, in the course of the bit stream.

20  
25 This is because the bit stream on which the transcoding is performed has the delay corresponding to the time necessary for the transcoding process as compared with the original bit stream. Also, this is because the simply switching operation can not be done

because of the difference of the bit stream structure caused by the encoding structure.

### Summary of the Invention

5           The present invention is accomplished in view of the above mentioned problems. Therefore, an object of the present invention is to provide a method and system for processing a video code, which can generate continuous moving pictures even when switching from a  
10 bit stream on which a transcoding is performed to an original bit stream, or from the original bit stream to the bit stream on which the transcoding is performed, in a course of the bit streams.

15           In order to achieve an aspect of the present invention, a video code processing method, includes:  
(a) providing a first original bit stream including a video code which is a digitized video signal; (b) generating a second original bit stream at a first timing by delaying the first original bit stream by a  
20 specific time interval; (c) generating a converted bit stream at a second timing, the first original bit stream being code-converted into the converted bit stream; and (d) switching between the second original bit stream and the converted bit stream to output, and  
25 wherein the specific time interval is adjusted such that the first timing is substantially equal to the second timing.

In this case, the specific time interval is adjusted such that continuous moving pictures corresponding to the first original bit stream can be obtained even when the (d) is performed in a course of the second original bit stream and the converted bit stream.

Also in this case, each of the second original bit stream and the converted bit stream has a plurality of frames, and wherein the (d) includes switching between the second original bit stream and the converted bit stream at a switching point corresponding to a start position or end position of one of the plurality of frames of the second original bit stream and the converted bit stream.

Further in this case, the first timing is determined by monitoring the second timing and controlling the specific time interval based on the monitoring result.

In this case, the first timing is determined by monitoring the first and second timings and controlling the specific time interval based on the monitoring result.

Also in this case, the first timing is determined by monitoring the first and second timings and performing feedback control on the specific time interval such that a difference between the first and second timings is reduced based on the monitoring

result.

Further in this case, the (d) includes switching between the second original bit stream and the converted bit stream at a switching point detected  
5 in accordance with a bit stream structure of an encoded picture of the first original bit stream.

In this case, the switching point is detected in accordance with a bit stream structure of an encoded picture of the first original bit stream such  
10 that continuous moving pictures corresponding to the first original bit stream can be obtained without a disturbance in the continuous moving pictures.

Also in this case, a video code processing method, further includes: (f) inputting a switch  
15 command at a third timing, and wherein each of the second original bit stream and the converted bit stream corresponds to MPEG (Moving Picture Experts Group) 2 type and has a plurality of GOPs (Group of Picture), each of the plurality of GOPs including an  
20 Intra-Picture (I Picture), a Predictive-Picture (P picture) and a Bidirectionally predictive-Picture (B picture), and wherein the (d) includes switching between the second original bit stream and the converted bit stream at a switching point  
25 corresponding to a lead position of one of the plurality of GOPs which is on the third timing or the closest to the third timing after the third timing.

In order to achieve another aspect of the present invention, a video code processing apparatus, includes: a buffer section inputting a first original bit stream including a video code which is a digitized video signal to generate a second original bit stream at a first timing by delaying the first original bit stream by a specific time interval; a transcoding section generating a converted bit stream at a second timing, the first original bit stream being code-converted into the converted bit stream; and a switching section switching between the second original bit stream and the converted bit stream to output, and wherein the specific time interval is adjusted such that the first timing is substantially equal to the second timing.

In this case, the specific time interval is adjusted such that continuous moving pictures corresponding to the first original bit stream can be obtained even when the switching section switches between the second original bit stream and the converted bit stream in a course of the second original bit stream and the converted bit stream.

Also in this case, each of the second original bit stream and the converted bit stream has a plurality of frames, and wherein the switching section switches between the second original bit stream and the converted bit stream at a switching point

corresponding to a start position or end position of one of the plurality of frames of the second original bit stream and the converted bit stream.

Further in this case, a video code processing  
5 apparatus, further includes: a buffer controlling section monitoring the second timing to control the specific time interval based on the monitoring result.

In this case, a video code processing apparatus,  
further includes: a buffer controlling section  
10 monitoring the first and second timings to control the specific time interval based on the monitoring result.

Also in this case, a video code processing  
apparatus, further includes: a buffer controlling  
section monitoring the first and second timings to  
15 perform feedback control on the specific time interval such that a difference between the first and second timings is reduced based on the monitoring result.

Further in this case, the switching section  
switches between the second original bit stream and  
20 the converted bit stream at a switching point detected in accordance with a bit stream structure of an encoded picture of the first original bit stream.

In this case, a video code processing apparatus,  
further includes: a switch controlling section  
25 inputting a switch command at a third timing to determine a switching point at which the switching section switches between the second original bit

stream and the converted bit stream, and wherein each  
of the second original bit stream and the converted  
bit stream corresponds to MPEG (Moving Picture Experts  
Group) 2 type and has a plurality of GOPs (Group of  
5 Picture), each of the plurality of GOPs including an  
Intra-Picture (I Picture), a Predictive-Picture (P  
picture) and a Bidirectionally predictive-Picture (B  
picture), and wherein the switch controlling section  
determines the switching point such that the switching  
10 point corresponds to a lead position of one of the  
plurality of GOPs which is on the third timing or the  
closest to the third timing after the third timing.

Also in this case, the buffer section and the  
transcoding section and the switching section are  
15 included in a single unit.

Further in this case, the buffer section and  
the transcoding section and the switching section and  
the buffer controlling section are included in a  
single unit.

20 In this case, the buffer section and the  
transcoding section and the switching section and the  
buffer controlling section and the switch controlling  
section are included in a single unit.

It is possible to output an encoded data in  
25 which screens of moving pictures are coincident since  
such a device tentatively holds therein an input  
original bit stream and then makes a timing of the

input original bit stream coincide with a timing of an output of a bit stream on which a transcoding is performed.

Moreover, since a switching controller is included, it is possible to accurately treat an encoded data corresponding to the same screen of a moving picture even for a bit stream structure of a different kind of an encode picture.

#### **Brief Description of the Drawings**

Fig. 1 is a function block diagram showing an embodiment of the present invention;

Fig. 2A is a timing chart showing a original bit stream inputted to a transcoder of Fig. 1;

Fig. 2B is a timing chart showing a converted bit stream outputted by the transcoder of Fig. 1;

Fig. 2C is a timing chart showing a original bit stream outputted by a buffer of Fig. 1;

Fig. 3 is a function block diagram showing an embodiment of the present invention, differently from Fig. 1;

Fig. 4A is a timing chart showing a original bit stream inputted to a transcoder of Fig. 3;

Fig. 4B is a timing chart showing a converted bit stream outputted by the transcoder of Fig. 3;

Fig. 4C is a timing chart showing a command outputted by a buffer controller of Fig. 3;

Fig. 4D is a timing chart showing a original bit stream outputted by the buffer of Fig. 3;

Fig. 5A is a timing chart showing a raw or converted bit stream of Fig. 3;

5 Fig. 5B is a timing chart showing a switch command inputted to the switch controller of Fig. 3; and

Fig. 5C is a timing chart showing a switch command outputted by the switch controller of Fig. 3.

#### **Description of the Preferred Embodiments**

An embodiment of the present invention will be described below with reference to the attached drawings.

15 Fig. 1 is a function block diagram showing an embodiment of the present invention. It is provided with a transcoder 1 and a buffer 2 for receiving a original bit stream to be inputted, and a switcher 3 for switching any one of outputs of the transcoder 1 and the buffer 2 and then connecting it to an external portion.

Fig. 1 is different from the conventional system for processing a video code, in a fact that the buffer 2 is mounted.

25 The transcoder 1 inputs the original bit stream A to convert into a converted bit stream B of a low rate, and outputs to the switcher 3. The buffer 2

inputs the original bit stream A to hold therein only  
for a period of the conversion in the transcoder 1,  
and outputs to the switcher 3. The switcher 3  
switches between the converted bit stream B outputted  
5 by the transcoder 1 and the original bit stream A  
outputted by the buffer 2, based on a switch command  
from the external portion, and outputs any one of the  
bit streams A, B to the external portion.

The operations of the function block in Fig. 1  
10 will be described below with reference to Figs. 1 and  
2A to 2C. Fig. 2A is a timing chart showing the  
original bit stream A inputted to the transcoder 1.  
Fig. 2B is a timing chart showing the converted bit  
stream B outputted by the transcoder 1. And, Fig. 2C  
15 is a timing chart showing the original bit stream A  
outputted by the buffer 2.

The converted bit stream B outputted by the  
transcoder 1 has a delay corresponding to a process  
time  $t_p$  in the transcoder 1, as compared with the  
20 original bit stream A inputted to the transcoder 1, as  
shown in Figs. 2A and 2B.

As shown in Figs. 2A and 2C, the buffer 2 holds  
therein the original bit stream A inputted to the  
transcoder 1 only for the process time  $t_p$ , and outputs  
25 it. Thus, in input sections of the switcher 3,  
respective frame positions of the converted bit stream  
B outputted by the transcoder 1 and the original bit

stream A outputted by the buffer 2 are in temporal coincidence with each other. The switcher 3 switches between the two input signals, namely, between the converted bit stream B on which the transcoding is performed and the original bit stream A outputted by the buffer 2, at a point such as a frame start or a frame end. As a result, it is possible to switch between the encode data without a disturbance in a moving picture.

An embodiment different from that of Fig. 1 will be described below with reference to Fig. 3. In Fig. 3, a system is provided with a transcoder 11, a buffer 12, a switcher 13, a buffer controller 14 and a switch controller 15.

Fig. 3 is different from Fig. 1 in a fact that the buffer controller 14 for controlling the buffer 12 and the switch controller 15 for controlling the switcher 13 are added.

The transcoder 11 has the function equal to the conventional function of converting the original bit stream A into the converted bit stream B of the low rate. The transcoder 11 outputs the converted bit stream B to the switcher 13, the buffer controller 14 and the switch controller 15.

The buffer 12 tentatively holds therein the original bit stream A under the control of the buffer controller 14, and outputs to the switcher 13, the

buffer controller 14 and the switch controller 15.

The switcher 13 receives the converted bit stream B outputted by the transcoder 11 and the original bit stream A outputted by the buffer 12, switches between the converted bit stream B and the original bit stream A, at a switch point between the frames, under the control of the switch controller 15, and outputs any one of the bit streams A, B to an external portion.

The buffer controller 14 receives the converted bit stream B from the transcoder 11 and the original bit stream A from the buffer 12. Based on the input signals A, B, the buffer controller 14 controls the buffer 12 so that the original bit stream A outputted by the buffer 12 is temporally equal to the converted bit stream B outputted by the transcoder 11 at the switch point between the frames.

The switch controller 15 receives the converted bit stream B outputted by the transcoder 11 or the original bit stream A outputted by the buffer 12, and controls the switcher 13 so as to switch at a timing suitable for the bit stream structure, based on a switch command inputted from the external portion.

The operations of the buffer controller 14 in Fig. 3 will be described below with reference to Fig. 3 and Figs. 4A to 4D.

The converted bit stream B outputted by the

transcoder 11 has a delay corresponding to a process time  $t_p$  in the transcoder 11, as compared with the original bit stream A inputted to the transcoder 11, as shown in Figs. 4A and 4B. The buffer 12

5 tentatively holds therein the original bit stream A, to output it, based on a command of the buffer controller 14 as shown in Figs. 4C and 4D.

As shown in Figs. 4B to 4D, the buffer controller 14 performs a control of holding and  
10 outputting the bit stream, on the buffer 12 so that the converted bit stream B outputted by the transcoder 11 is temporally equal to the original bit stream A outputted by the buffer 12. For example, the buffer controller 14 compares the original bit stream A  
15 outputted by the buffer 12 with the converted bit stream B outputted by the transcoder 11, and performs a feedback control on the buffer 12 so as to reduce a difference at a switch point between the frames to a small value, based on the comparison result.

20 The operations of the switch controller 15 in Fig. 3 will be described below with reference to Fig. 3 and Figs. 5A and 5B.

The switch controller 15 controls the switcher 13 so that the bit streams A, B are switched at an  
25 optimal timing. As the switch timing used in the switch controller 15, for example, when the bit streams corresponds to the MPEG2, it is possible to

use a unit of a group of pictures (GOP) composed of an intra encode picture (I-picture), an predictive encode picture (P-picture) and a bidirectionally predictive encode picture (B-picture) (refer to Fig. 5A).

5            Fig. 5A is a timing chart showing the converted bit stream B or the original bit stream A outputted by the buffer 12 which is received by the switch controller 15. Since the switch controller 15 receives the original bit stream A outputted by the  
10            buffer 12, an input timing of the original bit stream A is equal to that of the converted bit stream B. As mentioned above, the two timings of the bit streams A, B received by the switch controller 15 are equal to each other. So, from the viewpoint that it may be any  
15            timing of the two bit streams A, B, Fig. 5A shows the timing of the original bit stream A or the converted bit stream B.

            As shown in Figs. 5B and 5C, let us suppose that the switch controller 15 receives the switch  
20            command of the transcoding from a user or the system at a point  $T_i$ . The switch controller 15 detects a lead point  $T_s$  of a first GOP (refer to Fig. 5C) on and after the point  $T_i$  of Fig. 5B, in the original bit stream A outputted by the buffer 12 or the converted  
25            bit stream B on which the transcoding is performed as shown in Fig. 5A. Then, the switch controller 15 instructs the switcher 13 to carry out the switching

operation at the lead point  $T_s$ .

The switcher 13 will be described below by referring back to Fig. 3.

The switcher 13 switches to any one of the two  
5 input signals, namely, any one of the converted bit  
stream B on which the transcoding is performed and the  
original bit stream A outputted by the buffer 12, and  
connects it to an external output. In the MPEG2, all  
encoded pictures can be decoded for each the GOP.

10 Thus, any disturbance in the decoded pictures is never  
induced before and after the switching operation.

As mentioned above, the shortest switch point  
within the frame is selected for each of the bit  
stream structures of different kinds of encoded  
15 pictures. Thus, it is possible to accurately treat  
the encoded data corresponding to the same screen of  
the dynamic image in the shortest time, for the switch  
command (the switch command received at the point  $T_i$   
in the above-mentioned example) from the external  
20 portion. Hence, even in any of the bit stream  
structures, it is possible to switch between the  
original bit stream A and the converted bit stream B  
without the disturbance in the picture in the shortest  
time, for the switch command from the external portion.

25 Also, in the above-mentioned case, the buffer  
12 and the switcher 13 are explained as respective  
single members (units). However, instead of the

configuration, the transcoder 11 can contain therein the buffer function of the buffer 12 and the switch function of the switcher 13.

Here, the transcoder 11 containing therein the  
5 buffer function tentatively holds therein the original bit stream A until the original bit stream A is code-converted into the converted bit stream B, and then outputs the original bit stream A at the same timing as the output timing of the converted bit stream B.

10 Here, the transcoder 11 containing therein the switch function switches between the converted bit stream B and the original bit stream A having the same timing through the buffer function, based on the switch command from the external portion, and then  
15 outputs to the external portion.

The transcoder 11 containing therein the buffer function and the switch function as mentioned above can further contain therein the buffer control function of the buffer controller 14 as mentioned  
20 above. The transcoder 11 containing therein the buffer control function instructs the buffer function to make the output timings of both the bit streams B, A coincide with each other, based on the converted bit stream B and the original bit stream A outputted by  
25 the buffer function, and accordingly controls the tentatively held amount of the original bit stream A.

The transcoder 11 containing therein the buffer

function, the switch function and the buffer control function as mentioned above can further contain therein the switch control function of the switch controller 15 as mentioned above. The transcoder 11  
5 containing therein the switch control function detects the switch timing corresponding to the bit stream structure of any one encoded picture of both the bit streams B, A, based on the converted bit stream B and the original bit stream A outputted by the buffer  
10 function. After that, the transcoder 11, when receiving the switch command from the external portion, makes it coincide with the switch timing, and instructs the switch function, and then outputs any one of the converted bit stream B and the original bit  
15 stream A outputted by the buffer function.

In the above-mentioned explanation, the timing adjustment in the buffer is done at the frame unit, and the point of the switch control is defined as the GOP unit. However, another suitable unit may be  
20 selected depending on the configuration of the bit stream.

Also, the function blocks are illustrated and described. However, it is free to separate or merge the functions as long as the separation or the merger  
25 satisfies the above-mentioned functions. The above-mentioned explanations do not limit the present invention.

As mentioned above, the present invention can obtain the following effects.

The first effect lies in the fact that the continuous dynamic images can be generated even when  
5 switching from the bit stream on which the transcoding is performed to the original bit stream, in the course of the bit streams, or switching from the original bit stream to the bit stream on which the transcoding is performed in the course of the bit streams.

10 This is because it is possible to output the original bit stream at the same timing as the bit stream on which the transcoding is performed, by mounting the buffer function in the original bit stream to be inputted. As a result, the encoded data  
15 of the same dynamic image can be connected to the external output, even in any of the original bit stream and the bit stream on which the transcoding is performed.

The second effect lies in the fact that even in  
20 any of the bit stream structures, the switching operation can be done without the disturbance in the picture, in the shortest time, for the switch command from the external portion.

This is because it is possible to switch  
25 between the bit streams by selecting the optimal switch point from the bit stream structures based on the switch control function.

**What is claimed is:**

1. A video code processing method, comprising:

(a) providing a first original bit stream including a video code which is a digitized video signal;

5 (b) generating a second original bit stream at a first timing by delaying said first original bit stream by a specific time interval;

(c) generating a converted bit stream at a second timing, said first original bit stream  
10 being code-converted into said converted bit stream; and

(d) switching between said second original bit stream and said converted bit stream to output, and

15 wherein said specific time interval is adjusted such that said first timing is substantially equal to said second timing.

2. A video code processing method according to Claim 1, wherein said specific time interval is adjusted such that continuous moving pictures corresponding to said first original bit stream

5 can be obtained even when said (d) is performed in a course of said second original bit stream and said converted bit stream.

3. A video code processing method according to Claim 1, wherein each of said second original bit stream and said converted bit stream has a plurality of frames, and

5 wherein said (d) includes switching between said second original bit stream and said converted bit stream at a switching point corresponding to a start position or end position of one of said plurality of frames of said second original bit stream and said converted bit stream.

4. A video code processing method according to Claim 1, wherein said first timing is determined by monitoring said second timing and controlling said specific time interval based on the monitoring result.

5. A video code processing method according to Claim 1, wherein said first timing is determined by monitoring said first and second timings and controlling said specific time interval based on the monitoring result.

6. A video code processing method according to Claim 5, wherein said first timing is determined by monitoring said first and second timings and performing feedback control on said specific time

5 interval such that a difference between said first and second timings is reduced based on the monitoring result.

7. A video code processing method according to Claim 1, wherein said (d) includes switching between said second original bit stream and said converted bit stream at a switching point detected in accordance with a bit stream structure of an encoded picture of said first original bit stream.

8. A video code processing method according to Claim 7, wherein said switching point is detected in accordance with a bit stream structure of an encoded picture of said first original bit stream such that continuous moving pictures corresponding to said first original bit stream can be obtained without a disturbance in said continuous moving pictures.

9. A video code processing method according to Claim 1, further comprising:

(f) inputting a switch command at a third timing, and

5 wherein each of said second original bit stream and said converted bit stream corresponds to MPEG (Moving Picture Experts Group) 2 type and

has a plurality of GOPs (Group of Picture), each  
of said plurality of GOPs including an Intra-  
10 Picture (I Picture), a Predictive-Picture (P  
picture) and a Bidirectionally predictive-Picture  
(B picture), and

wherein said (d) includes switching between  
said second original bit stream and said converted  
5 bit stream at a switching point corresponding to a  
lead position of one of said plurality of GOPs  
which is on said third timing or the closest to  
said third timing after said third timing.

10. A video code processing apparatus,  
comprising:

a buffer section inputting a first original  
bit stream including a video code which is a  
5 digitized video signal to generate a second  
original bit stream at a first timing by delaying  
said first original bit stream by a specific time  
interval;

a transcoding section generating a  
10 converted bit stream at a second timing, said  
first original bit stream being code-converted  
into said converted bit stream; and

a switching section switching between said  
second original bit stream and said converted bit  
15 stream to output, and

wherein said specific time interval is adjusted such that said first timing is substantially equal to said second timing.

11. A video code processing apparatus according to Claim 10, wherein said specific time interval is adjusted such that continuous moving pictures corresponding to said first original bit stream can be obtained even when said switching section switches between said second original bit stream and said converted bit stream in a course of said second original bit stream and said converted bit stream.

12. A video code processing apparatus according to Claim 11, wherein each of said second original bit stream and said converted bit stream has a plurality of frames, and

wherein said switching section switches between said second original bit stream and said converted bit stream at a switching point corresponding to a start position or end position of one of said plurality of frames of said second original bit stream and said converted bit stream.

13. A video code processing apparatus according to Claim 10, further comprising:

a buffer controlling section monitoring  
said second timing to control said specific time  
5 interval based on the monitoring result.

14. A video code processing apparatus according  
to Claim 10, further comprising:

a buffer controlling section monitoring  
said first and second timings to control said  
5 specific time interval based on the monitoring  
result.

15. A video code processing apparatus according  
to Claim 10, further comprising:

a buffer controlling section monitoring  
said first and second timings to perform feedback  
5 control on said specific time interval such that a  
difference between said first and second timings  
is reduced based on the monitoring result.

16. A video code processing apparatus according  
to Claim 10, wherein said switching section  
switches between said second original bit stream  
and said converted bit stream at a switching point  
5 detected in accordance with a bit stream structure  
of an encoded picture of said first original bit  
stream.

17. A video code processing apparatus according to Claim 10, further comprising:

a switch controlling section inputting a switch command at a third timing to determine a switching point at which said switching section switches between said second original bit stream and said converted bit stream, and

wherein each of said second original bit stream and said converted bit stream corresponds to MPEG (Moving Picture Experts Group) 2 type and has a plurality of GOPs (Group of Picture), each of said plurality of GOPs including an Intra-Picture (I Picture), a Predictive-Picture (P picture) and a Bidirectionally predictive-Picture (B picture), and

wherein said switch controlling section determines said switching point such that said switching point corresponds to a lead position of one of said plurality of GOPs which is on said third timing or the closest to said third timing after said third timing.

18. A video code processing apparatus according to Claim 10, wherein said buffer section and said transcoding section and said switching section are included in a single unit.

19. A video code processing apparatus according to Claim 13, wherein said buffer section and said transcoding section and said switching section and said buffer controlling section are included in a single unit.

5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 113 114 115 116 117 118 119 120 121 122 123 124 125 126 127 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154 155 156 157 158 159 160 161 162 163 164 165 166 167 168 169 170 171 172 173 174 175 176 177 178 179 180 181 182 183 184 185 186 187 188 189 190 191 192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208 209 210 211 212 213 214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255 256 257 258 259 260 261 262 263 264 265 266 267 268 269 270 271 272 273 274 275 276 277 278 279 280 281 282 283 284 285 286 287 288 289 290 291 292 293 294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320 321 322 323 324 325 326 327 328 329 330 331 332 333 334 335 336 337 338 339 340 341 342 343 344 345 346 347 348 349 350 351 352 353 354 355 356 357 358 359 360 361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 388 389 390 391 392 393 394 395 396 397 398 399 400 401 402 403 404 405 406 407 408 409 410 411 412 413 414 415 416 417 418 419 420 421 422 423 424 425 426 427 428 429 430 431 432 433 434 435 436 437 438 439 440 441 442 443 444 445 446 447 448 449 450 451 452 453 454 455 456 457 458 459 460 461 462 463 464 465 466 467 468 469 470 471 472 473 474 475 476 477 478 479 480 481 482 483 484 485 486 487 488 489 490 491 492 493 494 495 496 497 498 499 500 501 502 503 504 505 506 507 508 509 510 511 512 513 514 515 516 517 518 519 520 521 522 523 524 525 526 527 528 529 530 531 532 533 534 535 536 537 538 539 540 541 542 543 544 545 546 547 548 549 550 551 552 553 554 555 556 557 558 559 560 561 562 563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585 586 587 588 589 590 591 592 593 594 595 596 597 598 599 600 601 602 603 604 605 606 607 608 609 610 611 612 613 614 615 616 617 618 619 620 621 622 623 624 625 626 627 628 629 630 631 632 633 634 635 636 637 638 639 640 641 642 643 644 645 646 647 648 649 650 651 652 653 654 655 656 657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673 674 675 676 677 678 679 680 681 682 683 684 685 686 687 688 689 690 691 692 693 694 695 696 697 698 699 700 701 702 703 704 705 706 707 708 709 710 711 712 713 714 715 716 717 718 719 720 721 722 723 724 725 726 727 728 729 730 731 732 733 734 735 736 737 738 739 740 741 742 743 744 745 746 747 748 749 750 751 752 753 754 755 756 757 758 759 760 761 762 763 764 765 766 767 768 769 770 771 772 773 774 775 776 777 778 779 780 781 782 783 784 785 786 787 788 789 790 791 792 793 794 795 796 797 798 799 800 801 802 803 804 805 806 807 808 809 810 811 812 813 814 815 816 817 818 819 820 821 822 823 824 825 826 827 828 829 830 831 832 833 834 835 836 837 838 839 840 841 842 843 844 845 846 847 848 849 850 851 852 853 854 855 856 857 858 859 860 861 862 863 864 865 866 867 868 869 870 871 872 873 874 875 876 877 878 879 880 881 882 883 884 885 886 887 888 889 890 891 892 893 894 895 896 897 898 899 900 901 902 903 904 905 906 907 908 909 910 911 912 913 914 915 916 917 918 919 920 921 922 923 924 925 926 927 928 929 930 931 932 933 934 935 936 937 938 939 940 941 942 943 944 945 946 947 948 949 950 951 952 953 954 955 956 957 958 959 960 961 962 963 964 965 966 967 968 969 970 971 972 973 974 975 976 977 978 979 980 981 982 983 984 985 986 987 988 989 990 991 992 993 994 995 996 997 998 999 1000

20. A video code processing apparatus according to Claim 17, wherein said buffer section and said transcoding section and said switching section and said buffer controlling section and said switch controlling section are included in a single unit.

### Abstract of the Disclosure

A video code processing method includes (a), (b), (c) and (d). The (a) step includes providing a first original bit stream including a video code which is a digitized video signal. The (b) step includes generating a second original bit stream at a first timing by delaying the first original bit stream by a specific time interval. The (c) step includes generating a converted bit stream at a second timing. The first original bit stream is code-converted into the converted bit stream. The (d) step includes switching between the second original bit stream and the converted bit stream to output. The specific time interval is adjusted such that the first timing is substantially equal to the second timing.

Fig. 1

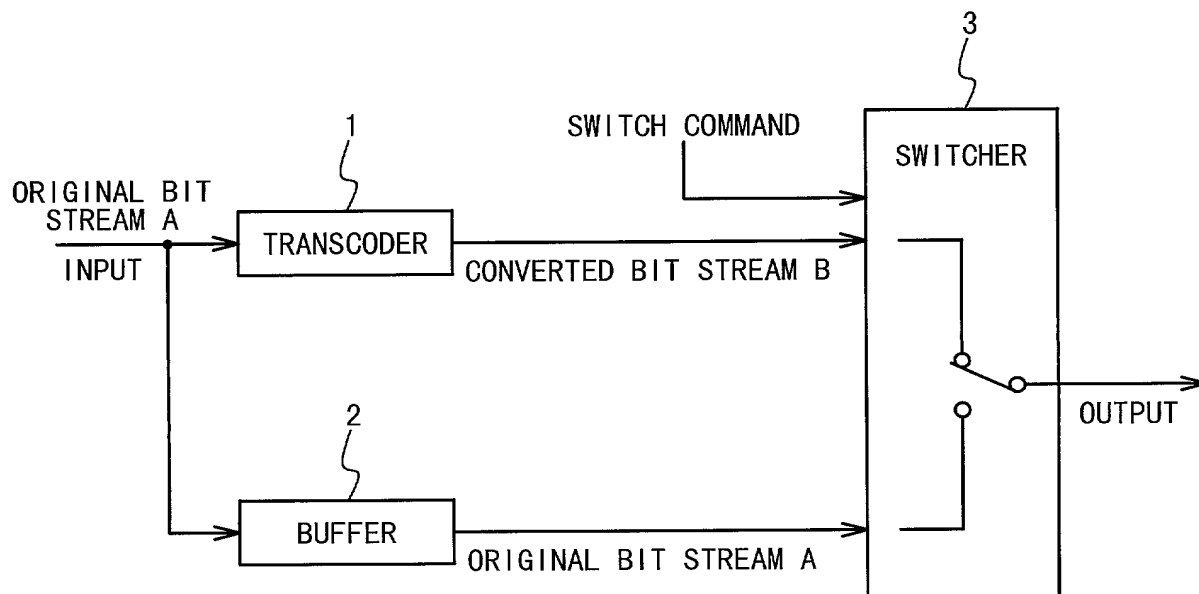


Fig. 2A

INPUTTED ORIGINAL BIT STREAM A

	A1	A2	A3	...
--	----	----	----	-----

Fig. 2B

CONVERTED BIT STREAM B  
OUTPUTTED BY TRANSCODER 1

	B1	B2	B3	...
--	----	----	----	-----

Fig. 2C

ORIGINAL BIT STREAM A  
OUTPUTTED BY BUFFER 2

	A1	A2	A3	...
--	----	----	----	-----

F i g . 3

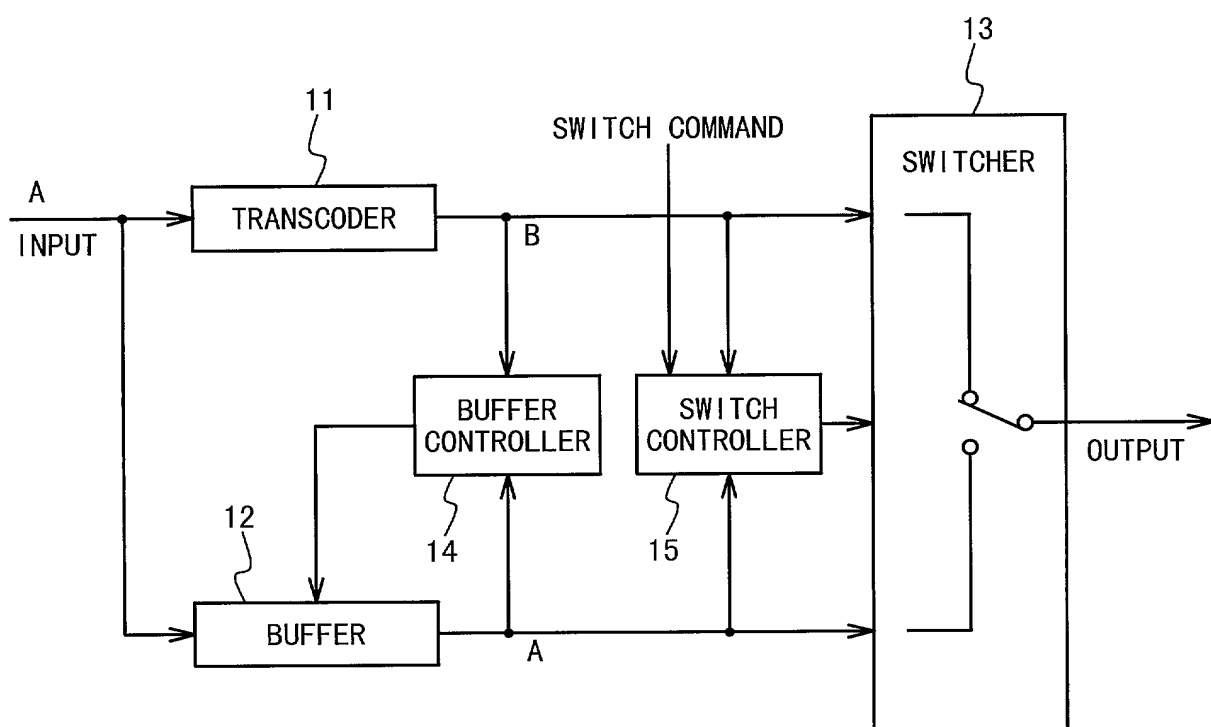


Fig. 4A

INPUTTED ORIGINAL BIT STREAM A

	A1	A2	A3	...
--	----	----	----	-----

Fig. 4B

CONVERTED BIT STREAM B  
OUTPUTTED BY TRANSCODER 11

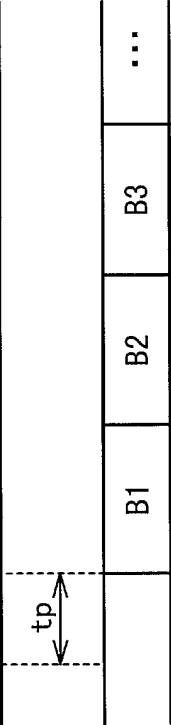


Fig. 4C

BUFFER CONTROLLER 14



Fig. 4D

ORIGINAL BIT STREAM A  
OUTPUTTED BY BUFFER 12

	A1	A2	A3	...
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Fig. 5A

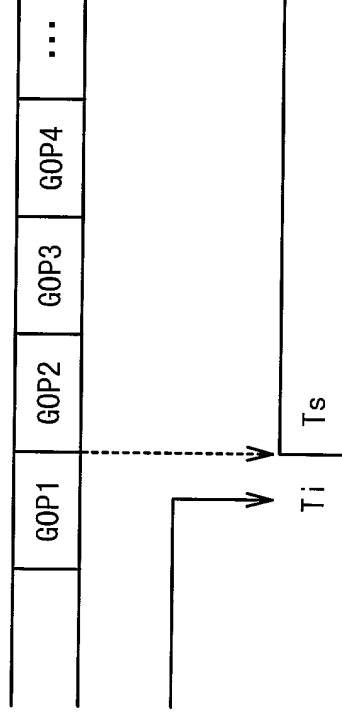
ORIGINAL OR CONVERTED BIT STREAM

Fig. 5B

SWITCH COMMAND

Fig. 5C

SWITCH CONTROLLER 15



0045FP529

UNITED STATES OF AMERICA COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION			OFGS FILE NO. P/2635-55
<p>As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named) of the subject matter which is claimed and for which a patent is sought on the invention entitled:</p> <p><b>A VIDEO CODE PROCESSING METHOD, WHICH CAN GENERATE CONTINUOUS MOVING PICTURES</b></p>			
<p>the specification of which is attached hereto, unless the following box is checked:</p> <p><input type="checkbox"/> was filed on _____ as United States patent Application Number or PCT International patent application number _____ and was amended on _____ (if any).</p>			
<p>I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.</p> <p>I acknowledge the duty to disclose all information known to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.</p> <p>I hereby claim priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate or United States provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:</p>			
Prior Foreign or Provisional Application(s)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. 119
Japan	301227/1999	22, 10, 1999	YES <input checked="" type="checkbox"/> NO <input type="checkbox"/>
			YES <input type="checkbox"/> NO <input type="checkbox"/>
			YES <input type="checkbox"/> NO <input type="checkbox"/>
<p>I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.</p>			
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<p>I hereby appoint customer no. 2352 OSTROLENK, FABER, GERB &amp; SOFFEN, LLP, and the members of the firm, Samuel H. Weiner - Reg. No. 18,510; Jerome M. Berliner - Reg. No. 18,653; Robert C. Faber - Reg. No. 24,322; Edward A. Meilman - Reg. No. 24,735; Stanley H. Lieberstein - Reg. No. 22,400; Steven I. Weisburd - Reg. No. 27,409; Max Moskowitz - Reg. No. 30,576; Stephen A. Soffen - Reg. No. 31,063; James A. Finder - Reg. No. 30,173; William O. Gray, III - Reg. No. 30,944; Louis C. Dujmich - Reg. No. 30,625 and Douglas A. Miro - Reg. No. 31,643, as attorneys with full power of substitution and revocation to prosecute this application, to transact all business in the Patent &amp; Trademark Office connected therewith and to receive all correspondence.</p>			
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